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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,220	11/19/2003	Sadeg M. Faris		6028

26665 7590 05/05/2005

REVEO, INC.
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ELMSFORD, NY 10523

EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/717,220	FARIS, SADEG M.
	Examiner	Art Unit
	Chuong A. Luu	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *21-23 and 46-48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 24-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of Group I, claims 1-20 and 26-45 in the reply filed on February 28, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The Rejections

Claims 1-6, 9-23, 26-31 and 34-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Sickmiller (U.S. 6,214,733 B1).

Sickmiller discloses a semiconductor device with

(1); (15); (26) providing a bulk substrate (14);

selectively creating strong bond regions and weak bond regions on said substrate (see column 7, lines 55-65; column 8, lines 35-44);

providing a first bond semiconductor layer (24) vertically supported on said substrate (14);

creating an electrode (20) on said first bond semiconductor layer (24), said electrodes (20) corresponding to said weak bond regions;

creating an actuatable element disposed opposite said electrode;

removing said first semiconductor layer from said bulk substrate;

bonding said first semiconductor layer to a second semiconductor layer (see Figures 1-6);

(2) further comprising the step of aligning said first semiconductor layer with said second semiconductor layer having similarly positioned electrodes (see Figure 2);

(3); (28) wherein said aligning step is mechanical alignment (see column 3, lines 44-50);

(4); (29) wherein said aligning step is optical alignment (see column 9, lines 49-55);

(5) further comprising the step of creating an electrode on said second semiconductor layer (see Figure 2);

(6) wherein said second semiconductor layer semiconductor device portions on said weak bond regions (see column 7, lines 55-65; column 8, lines 35-44);;

(9) further comprising the step of interconnecting said first semiconductor layer with said second semiconductor layer (see Figures 7-9);

(10) wherein said step of interconnecting is implemented at the edge of said semiconductor layers (see Figures 7-9);

(11) wherein said step of interconnecting is electrically coupling (see Figures 7-9);

(12) wherein said step of interconnecting is optically coupling (see Figures 7-9);

(13) wherein said step of interconnecting is performed vertically through said semiconductor layers (see Figures 1-9);

(14) further comprising the steps of: removing said second semiconductor layer from said bulk substrate; bonding said second semiconductor layer to said first semiconductor layer (see Figures 1-9);

(16) wherein MEMs devices are formed from any two of the said N semiconductor layers (see Figure 1);

(17) further comprising the step of dicing said boned semiconductor layers to form one or more dies (see Figure 2);

(18) further comprising the step of: interconnecting said bonded semiconductor layers after dicing step (see Figures 1-9);

(19) further comprising the step of: forming edge connectors on the boundary of said one or more dies (see Figures 1-9);

(20) wherein said edge connector serve as diagnostic conductors to determine health of individual die layers (see Figures 1-9);

(27) further comprising the step of aligning said first layer with said second layer having similarly positioned ports (see Figures 1-9);

(30) further comprising the step of creating a port on said second layer (see Figures 1-9);

(31) wherein said second layer has microfluidic device portion on said weak bond regions (see Figures 1-9);

(34) further comprising the step of interconnecting said first layer with said second layer (see Figures 1-9);

(35) wherein said step of interconnecting is implemented at the edge of said first and said second layers (see Figures 1-9);

(36) wherein said step of interconnecting is performed vertically through said first and said second layers (see Figures 1-9);

(37) further comprising the steps of: removing said second layer from said bulk substrate;

bonding said second layer to said first layer (see Figures 1-9);

(38) further comprising the steps of: providing an Nth layer vertically supported on said bulk substrate, said Nth layer having strong bond regions and weak bond regions;

creating a port on said Nth layers, said port corresponding to said weak bond regions;

removing said Nth layer from said bulk substrate;

bonding said Nth layer to an (N-1) layer;

(39) wherein miorofluidic devices are formed from any two of said N layers (see Figures 1-9);

(40) further comprising the step of: dicing said bonded layer to form one or more dies (see Figures 1-9);

(41) further comprising the step of: interconnecting said bonded layers after said dicing layer (see Figures 1-9);

(42) further comprising the step of: forming edge connector on the boundary of said one or mote dies (see Figures 1-9);

(43) wherein said edge connectors serve as diagnostic indicators for determining the health of individual die layers (see Figures 1-9).

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 7-8 and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sickmiller (U.S. 6,214,733 B1).

Sickmiller does not explicitly disclose the ratio of area of said strong bond regions to said weak bond regions is greater than 1. It would advantageously provide a good

protection of the semiconductor device and low the metal diffusion to the substrate. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the ratio of area of said strong bond regions to said weak bond regions is greater than 1 of Sickmiller 's devices within the range as claimed for the purpose of obtaining the better performance of a semiconductor device, and it also has been held that where the general conditions of a claim are disclosed in the prior ad, discovering the optimum or workable ranges involves only routine skill in the art and it is noted that the applicant does not disclose criticality in the ranges claimed. In re Aller, 105 USPQ 233 (see MPEP 2144.05). Also, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Claims 24-25 and 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sickmiller (U.S. 6,214,733 B1) in view of Zavracky et al. (U.S. 5,976,953).

Sickmiller teaches the above outlined features except for wherein said bulk substrate includes a buried oxide layer, which is formed by ion implantation. However, Zavracky discloses a semiconductor device with **(24); (44)** wherein said bulk substrate includes a buried oxide layer (see column 13, lines 22-27); **(25); (45)** wherein said buried oxide layer is formed by ion implantation (see column 13, lines 22-27). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sickmiller (accordance

with the teaching of Zavracky). Doing so would facilitate the manufacture of the semiconductor device and increase the speed of the device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Patent Examiner
April 27, 2005